



Fig. 1

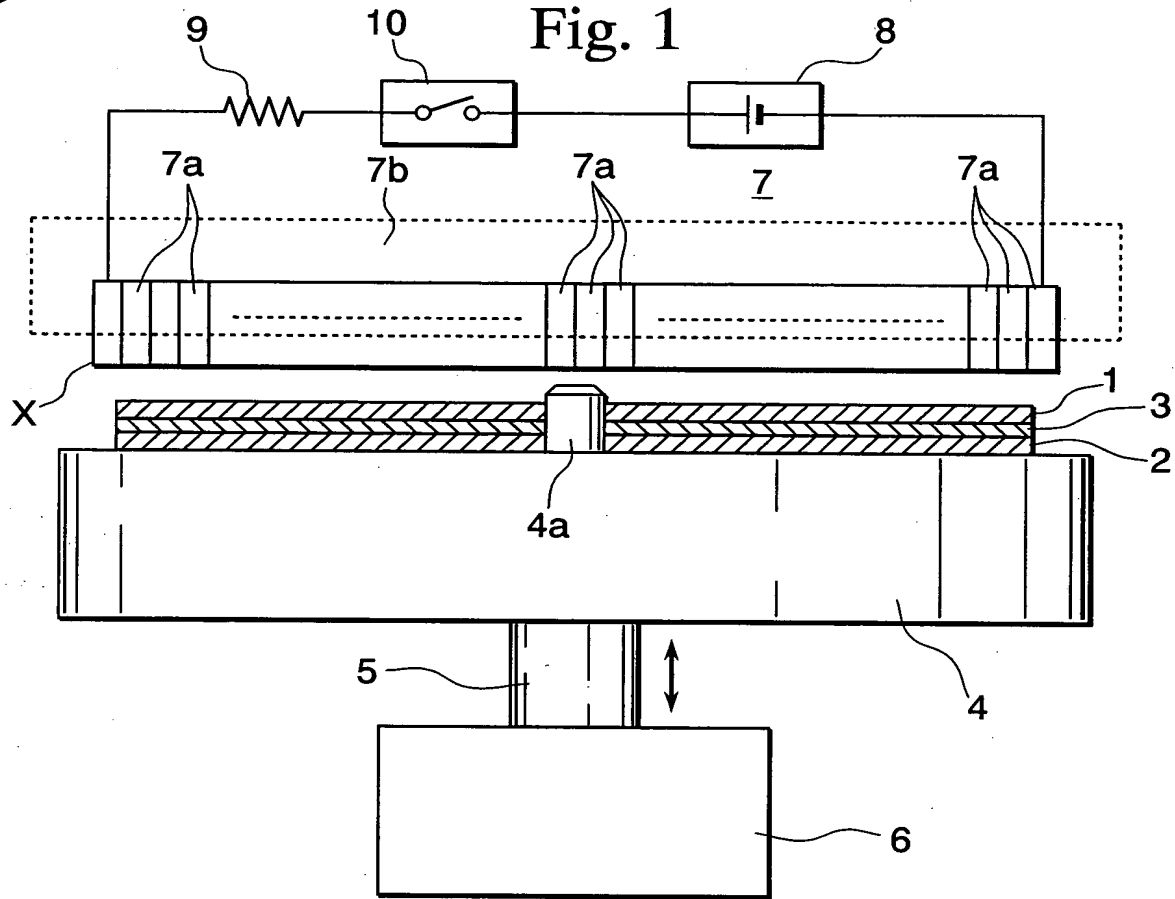


Fig. 2

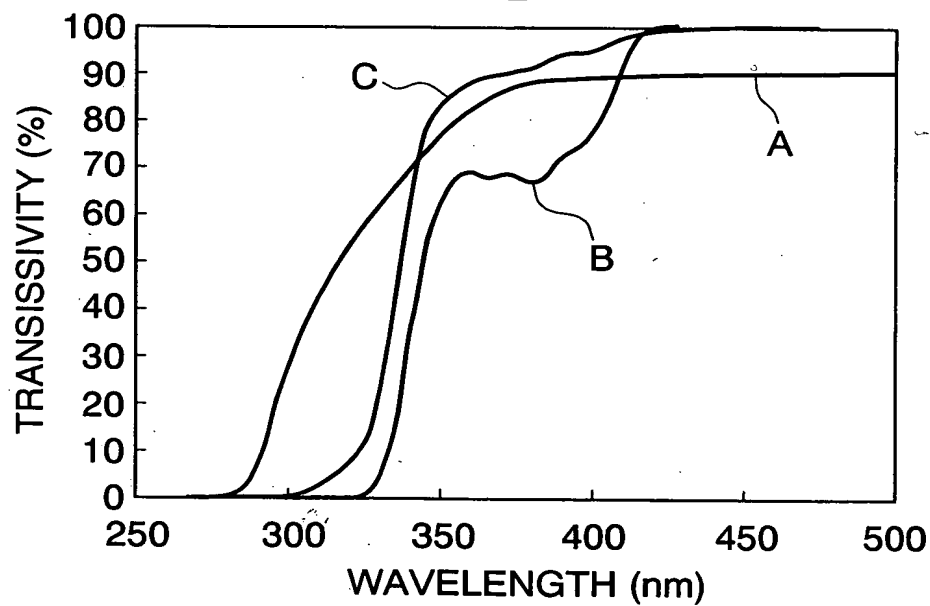


Fig. 3

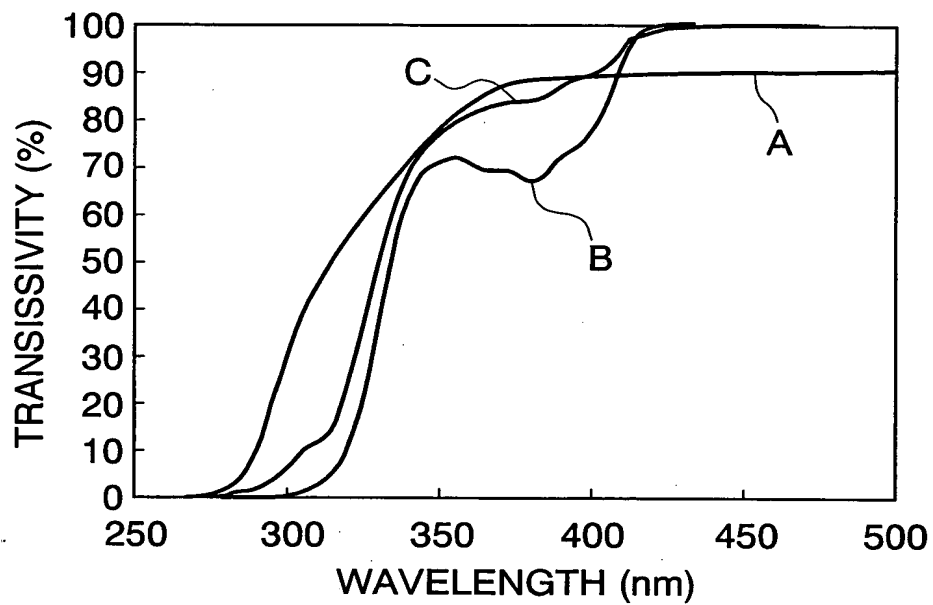


Fig. 4

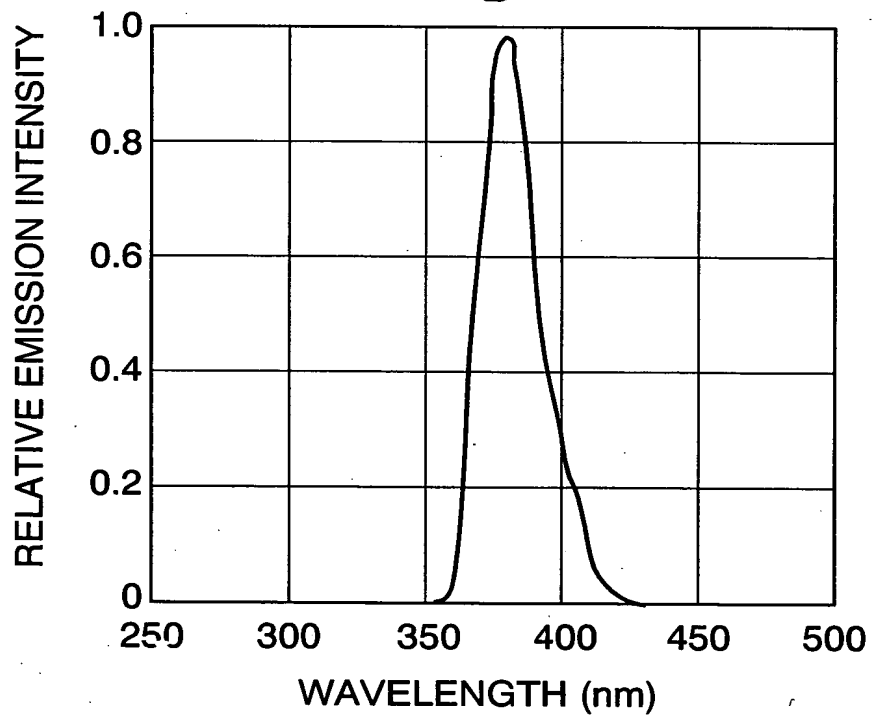


Fig. 5

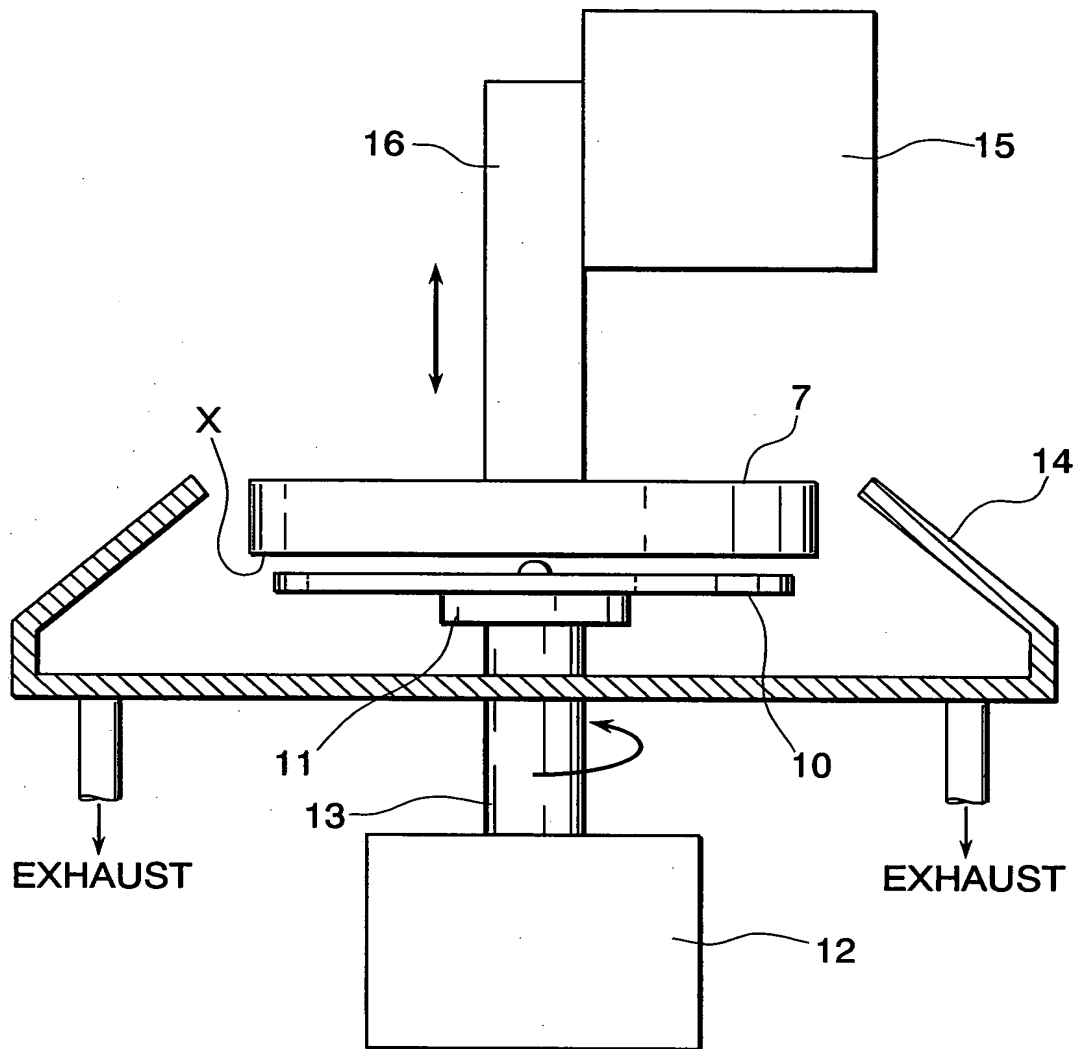


Fig. 6A

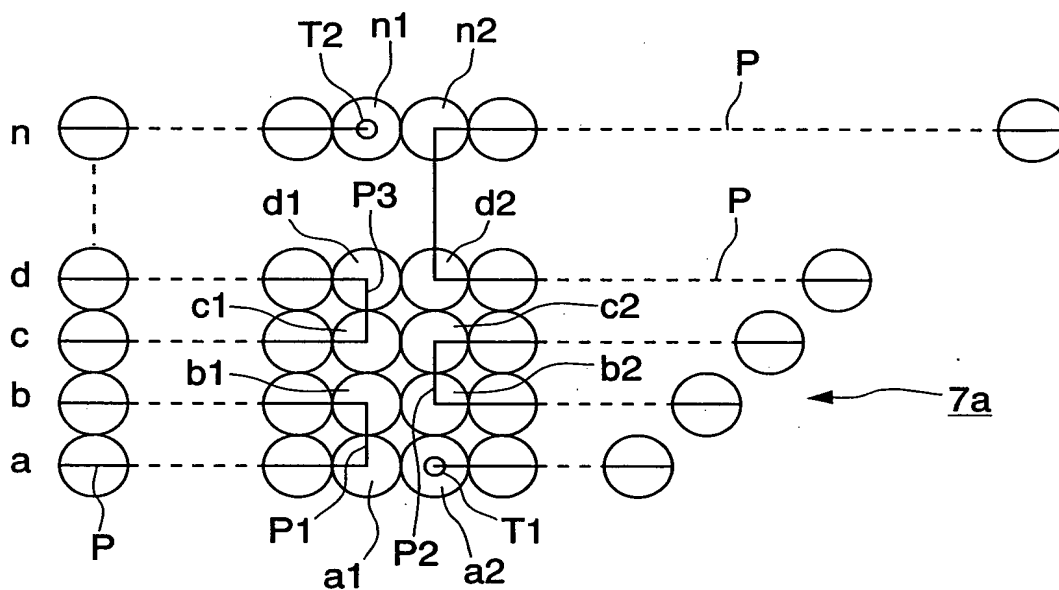


Fig. 6B

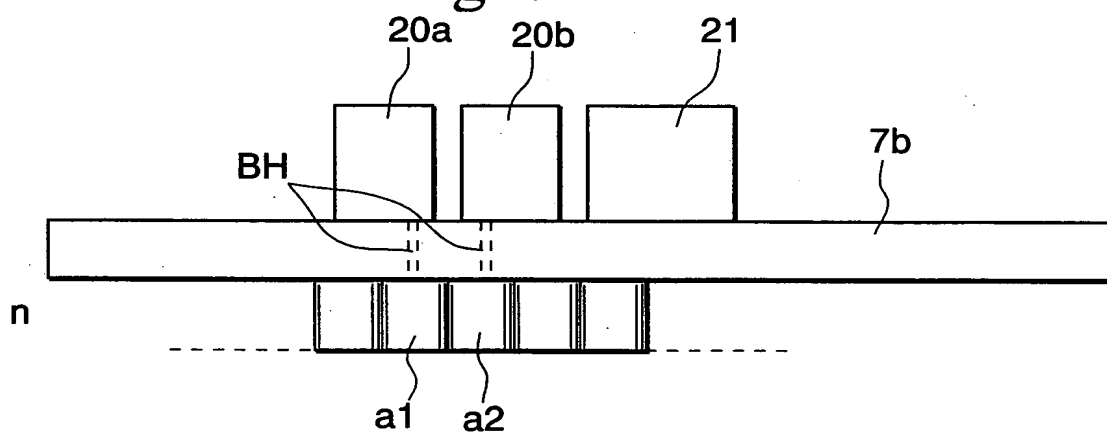


Fig. 7A

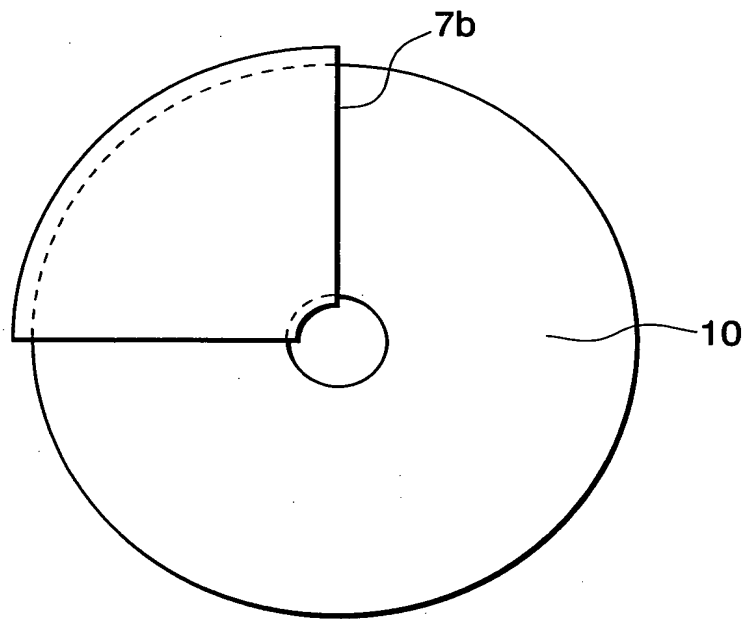


Fig. 7B

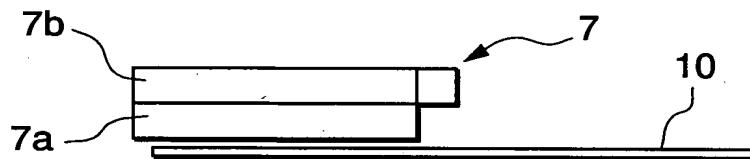


Fig. 8

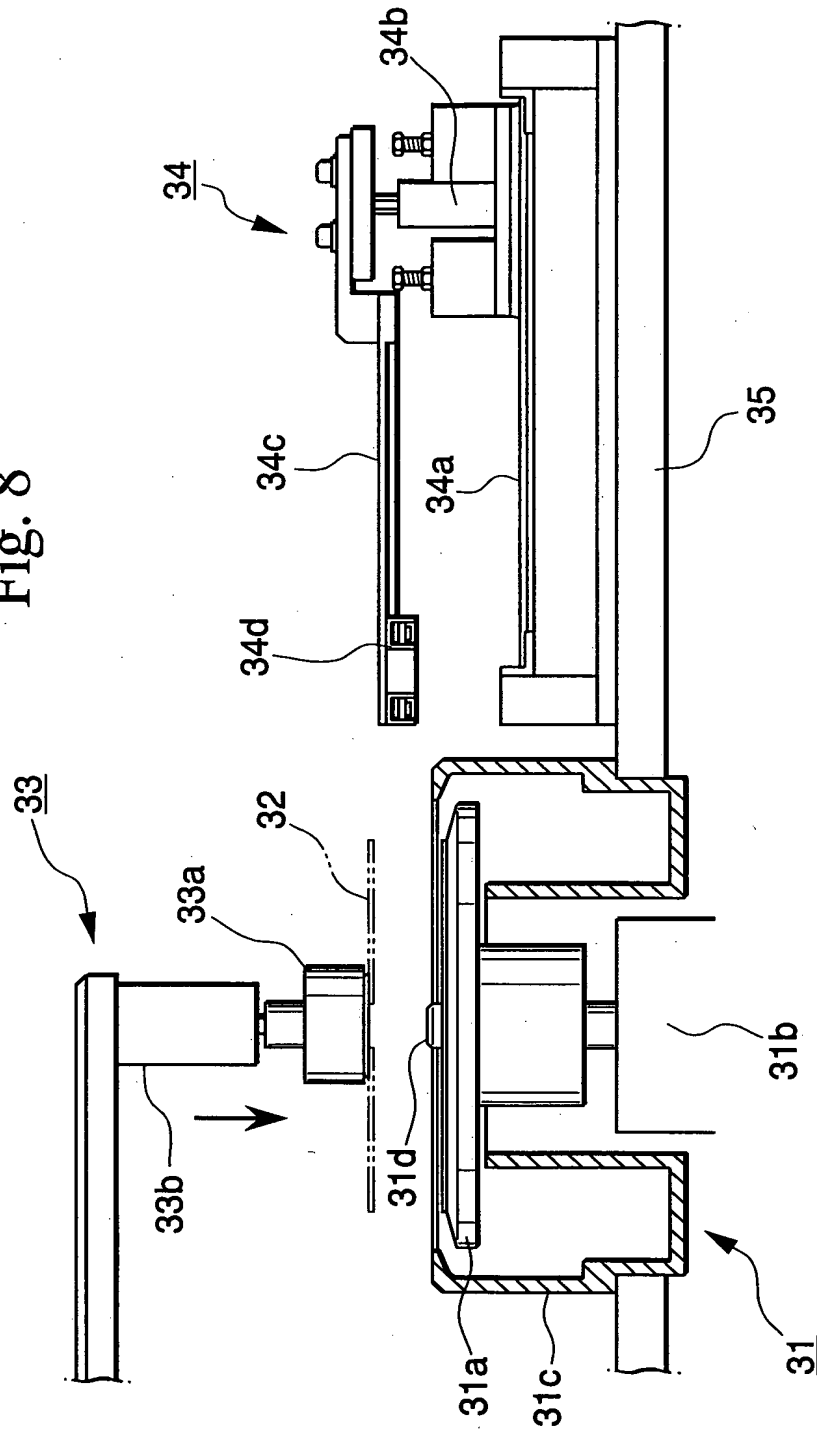
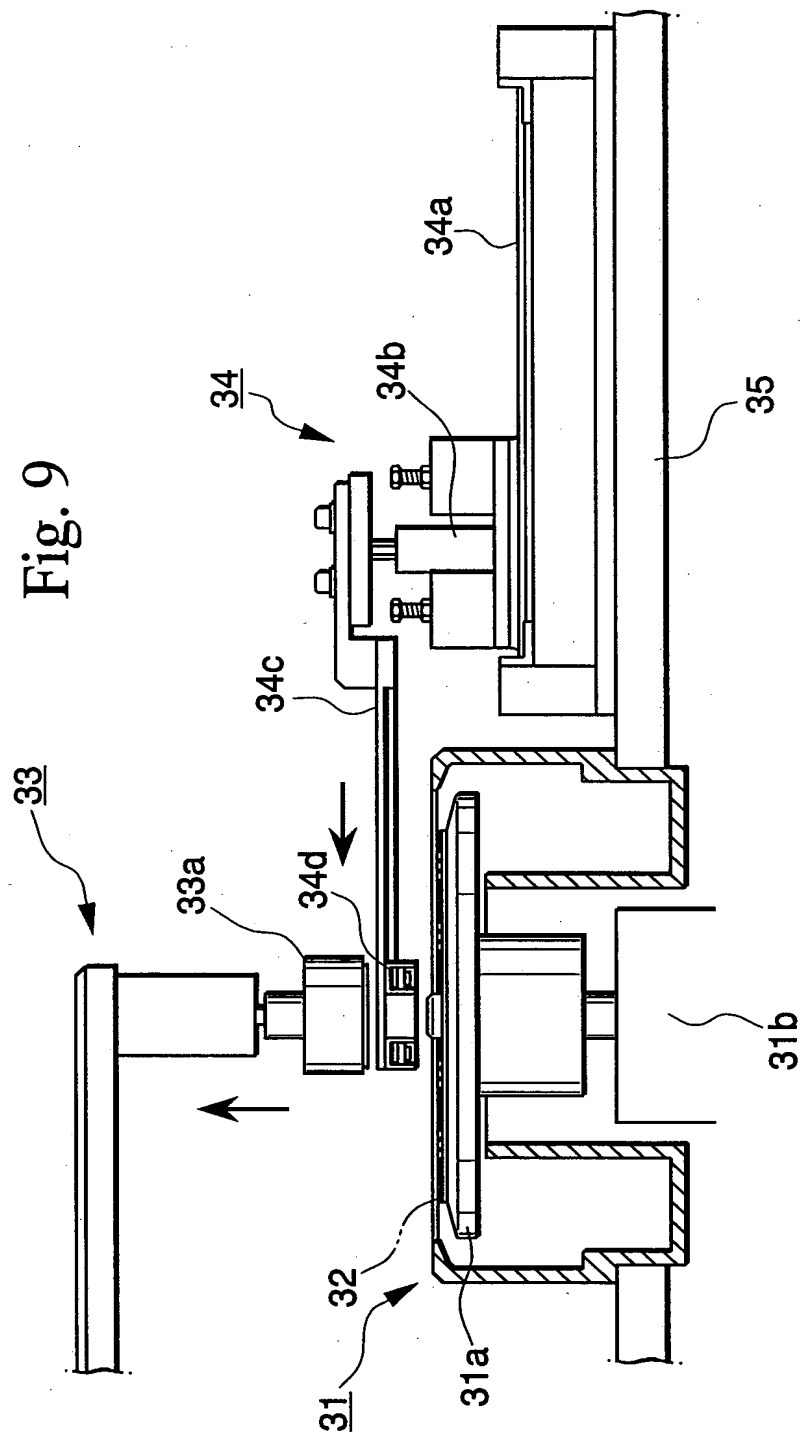


Fig. 9



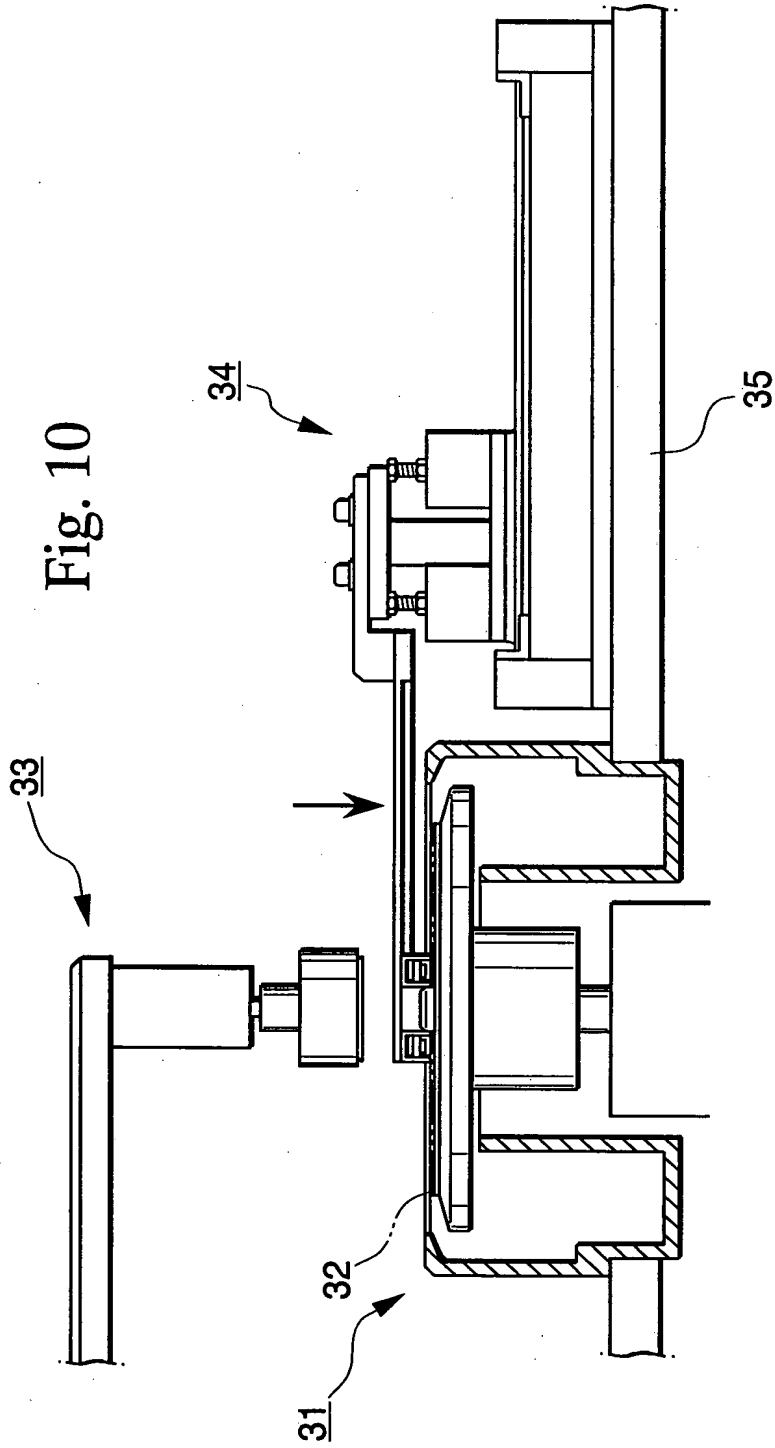




Fig. 11

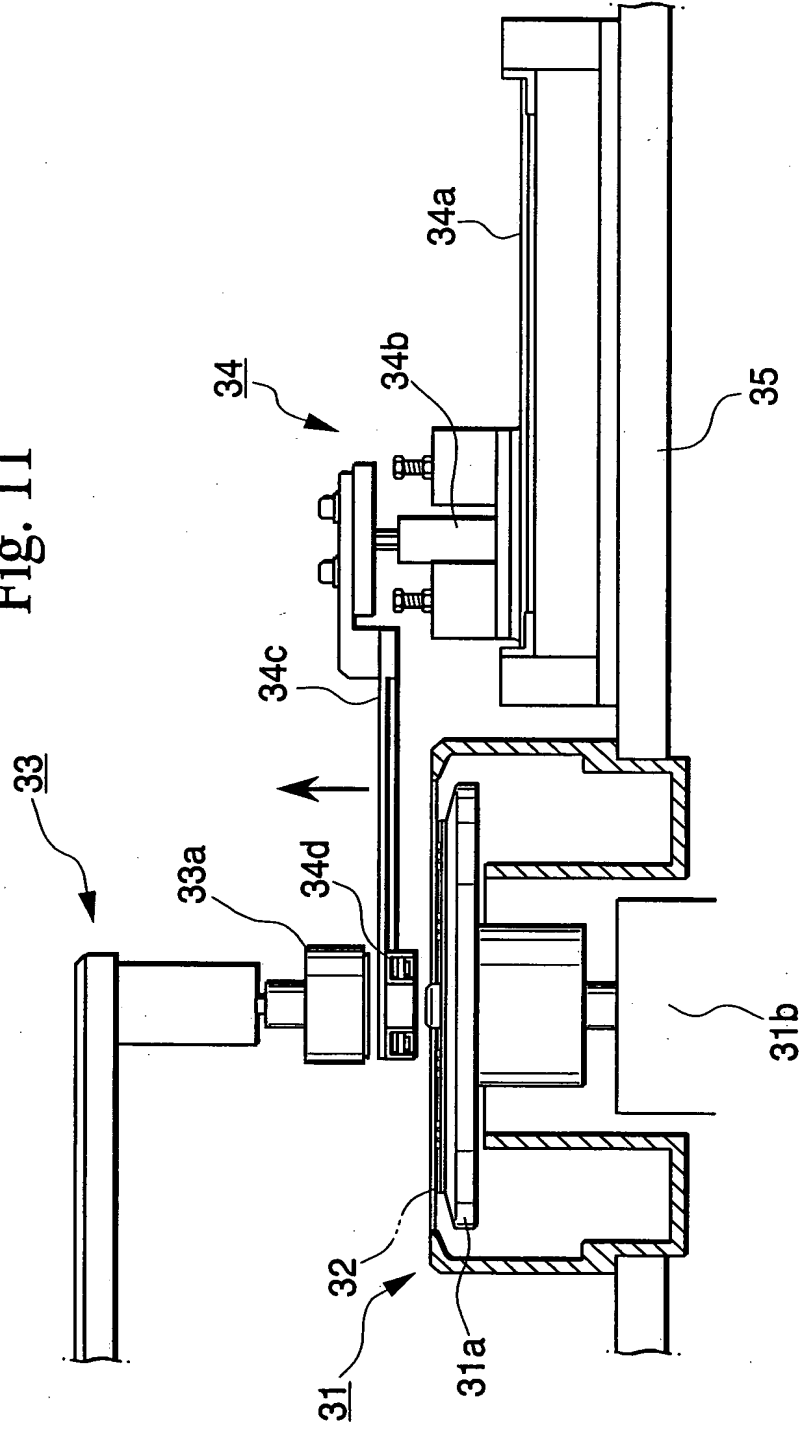
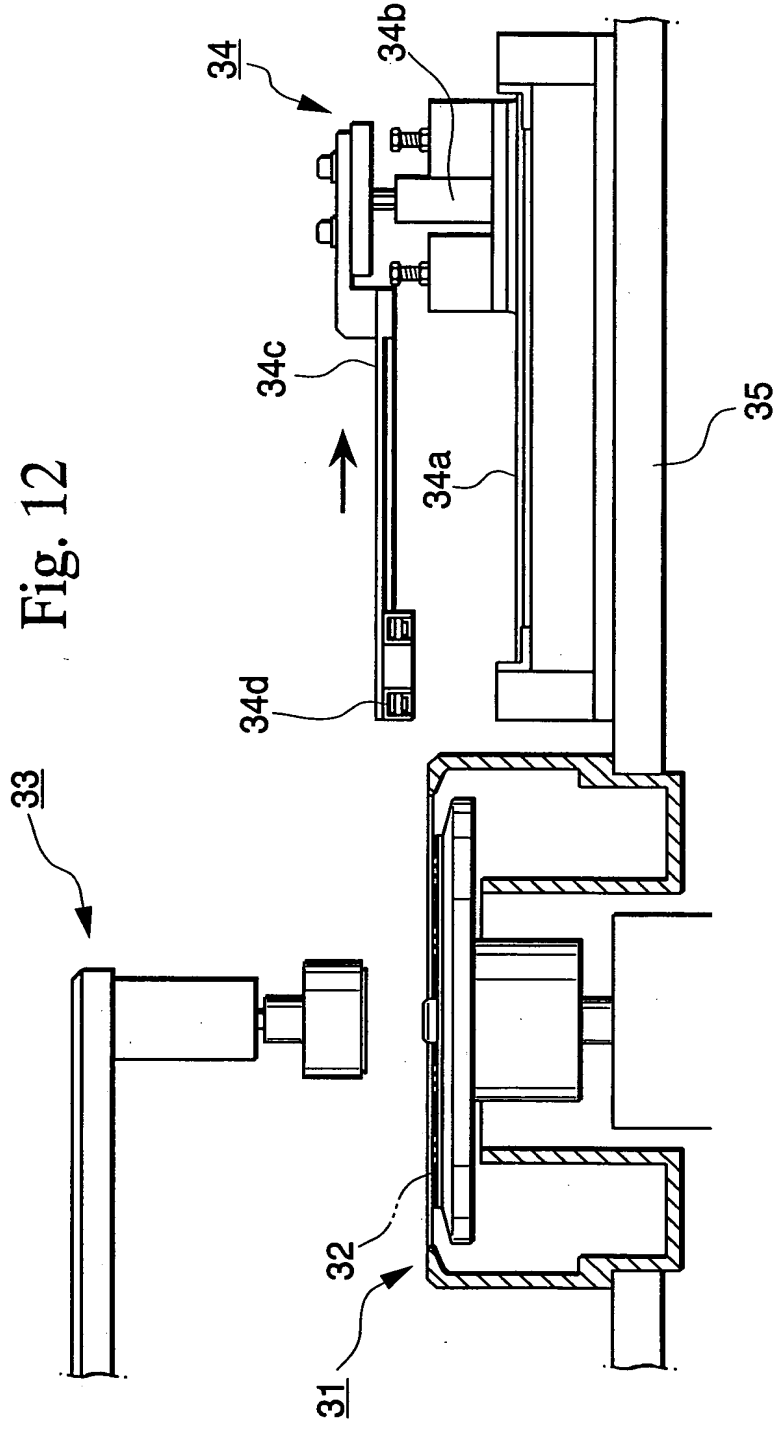
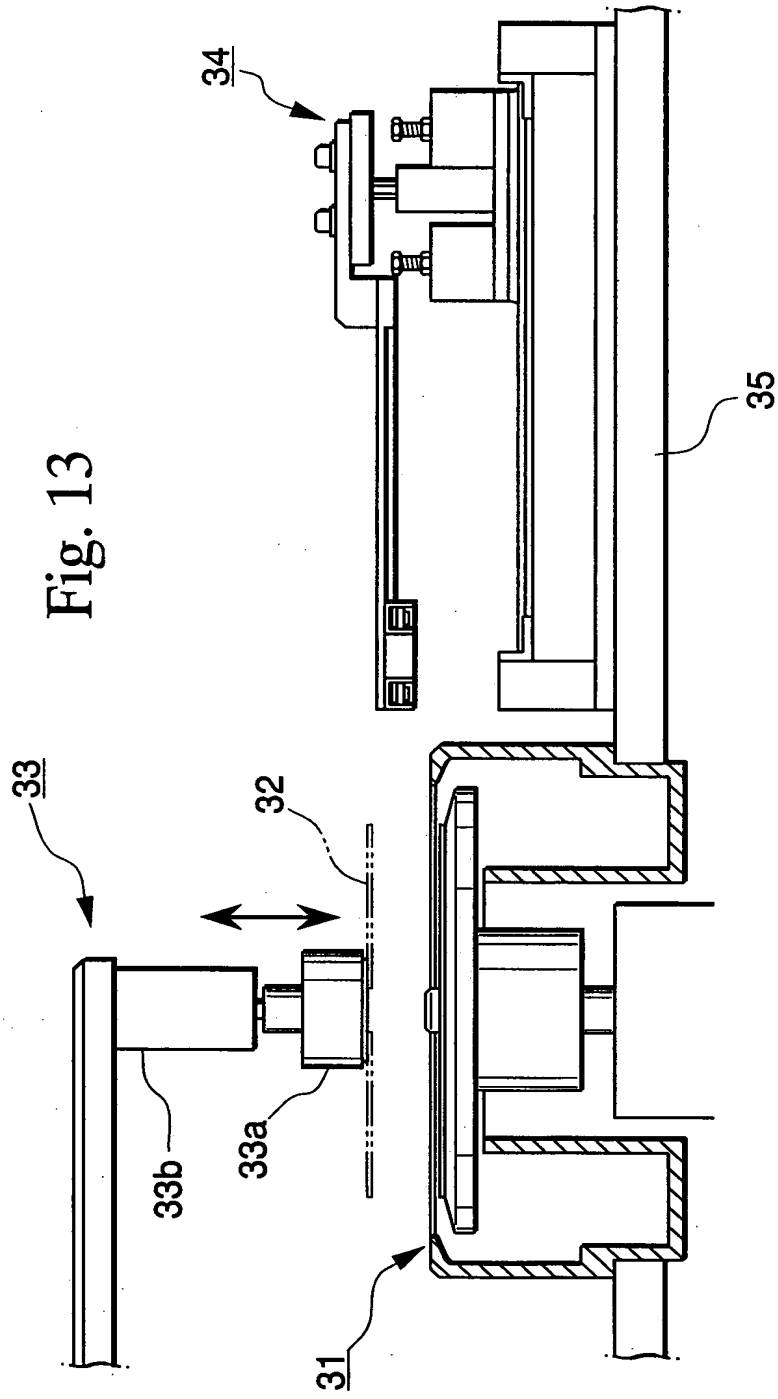


Fig. 12





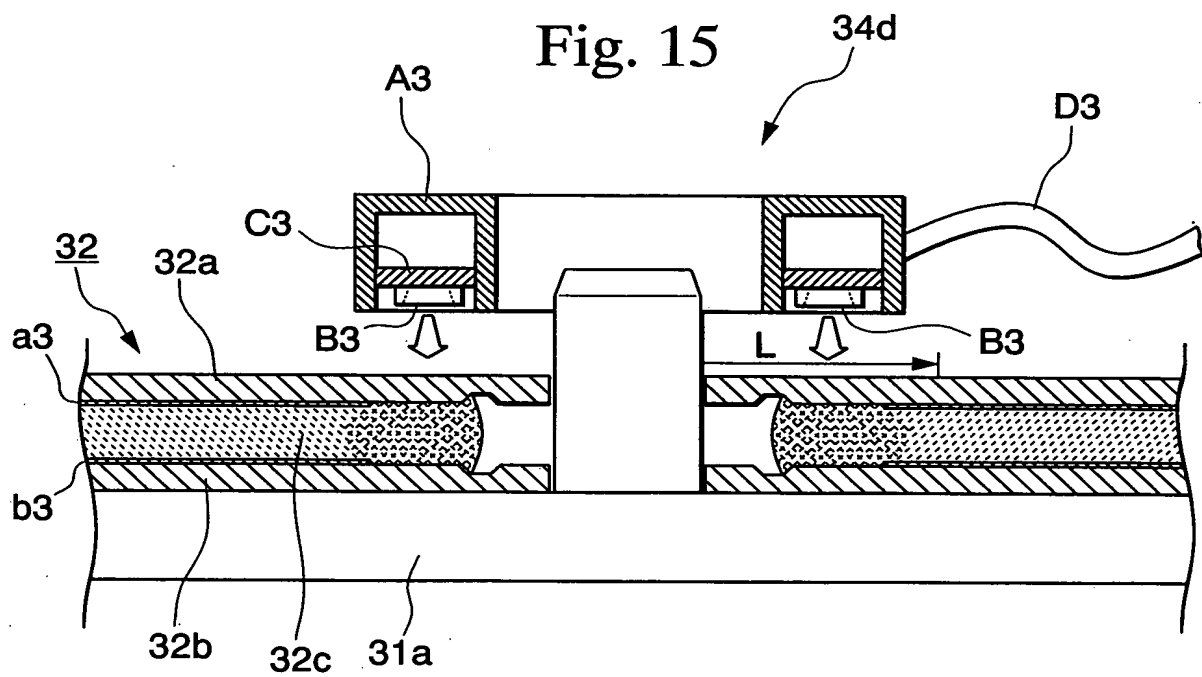
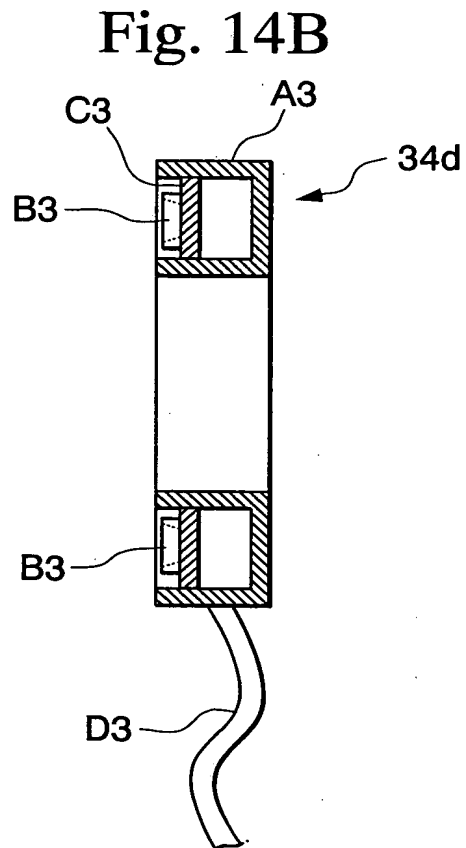
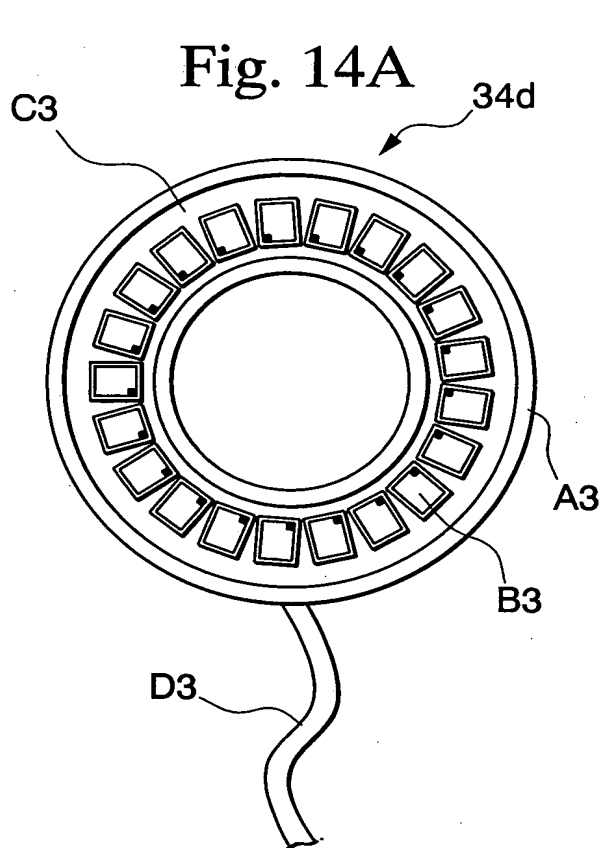


Fig. 16

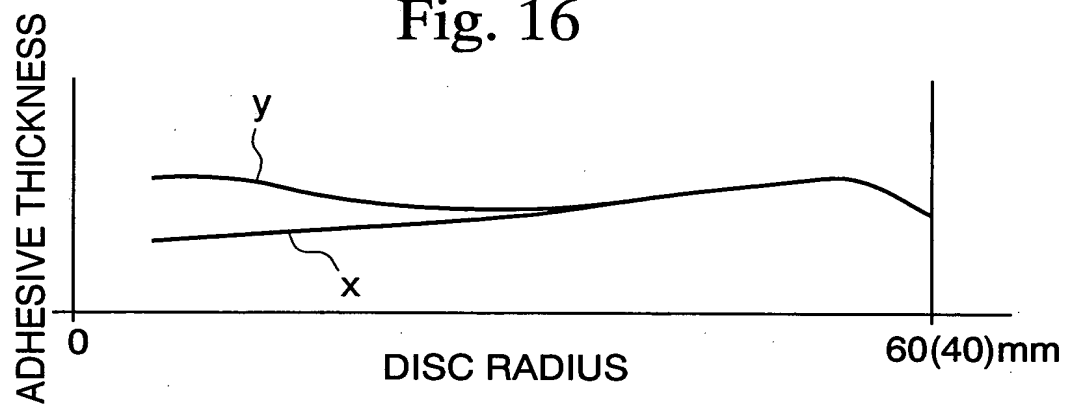


Fig. 17A

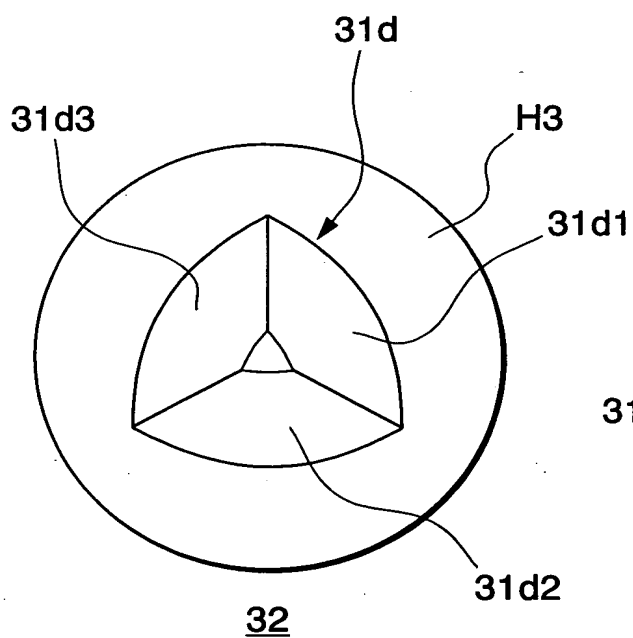
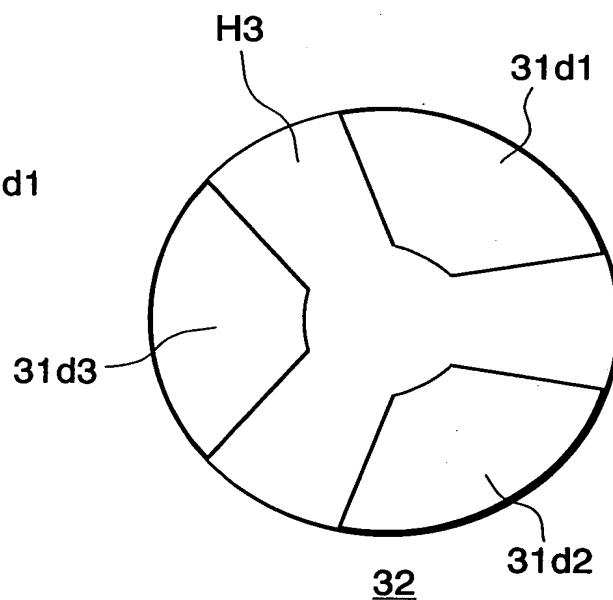


Fig. 17B



A cross-sectional view of a semiconductor device. A central pillar (44) is positioned between two side regions (41a and 41b). The side regions (41a, 41b) contain a central layer (42) and a lower layer (41b). A distance L is indicated between the central pillar and the side regions. The device is mounted on a substrate (43) with a base layer (411b). Various components are labeled with reference numerals: 416a, 416b, 41a, 42, 41b, 411b, 410, 48, 45, 46, 47, and 43.

Fig. 20

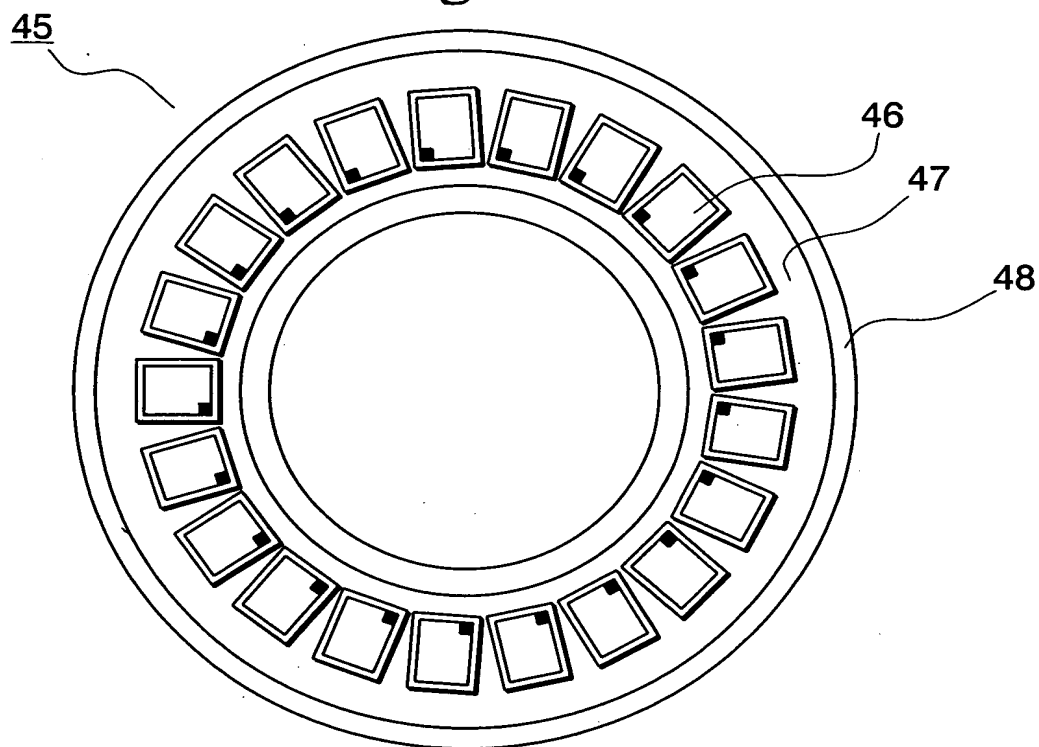


Fig. 21

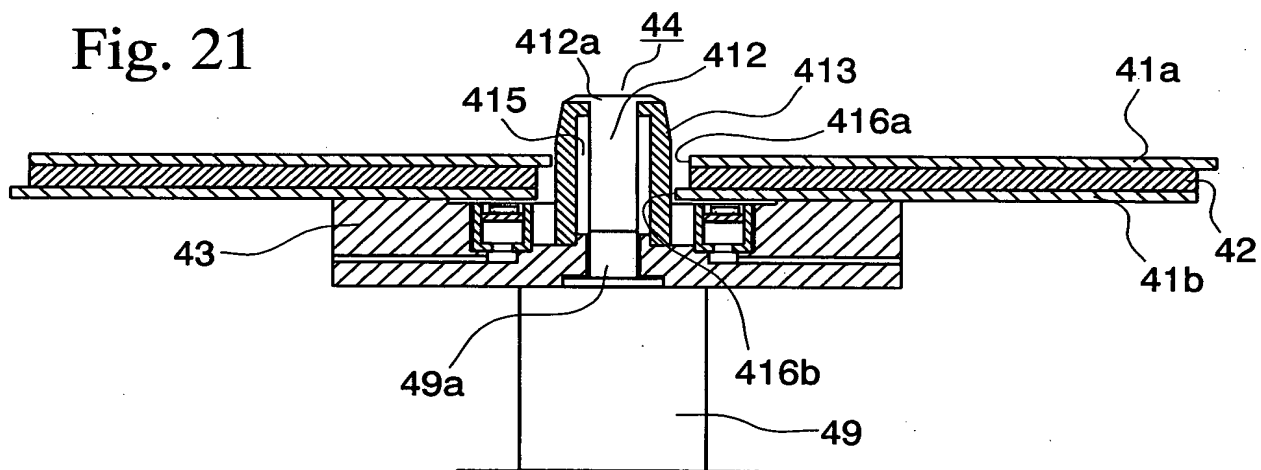


Fig. 22

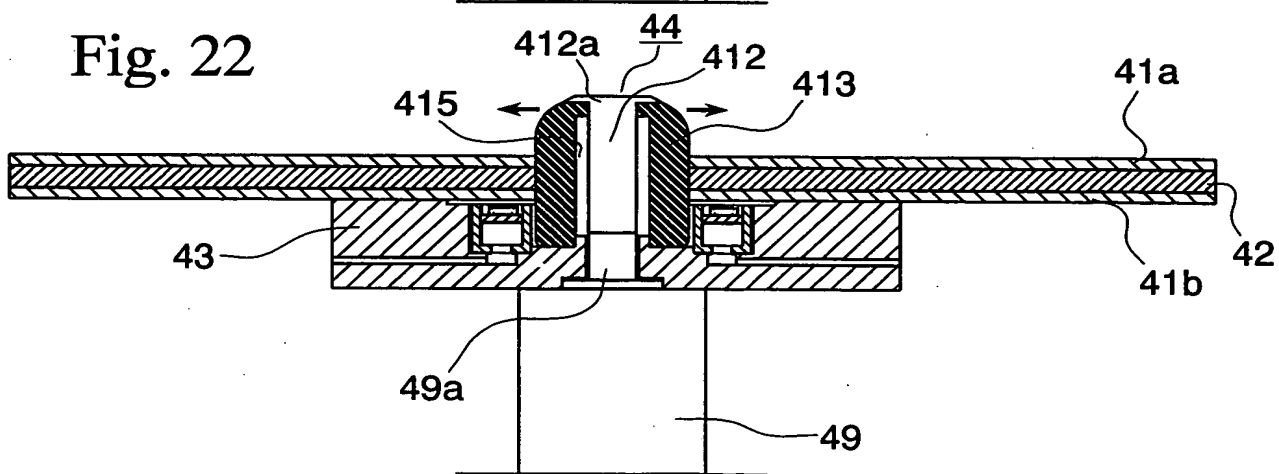


Fig. 23

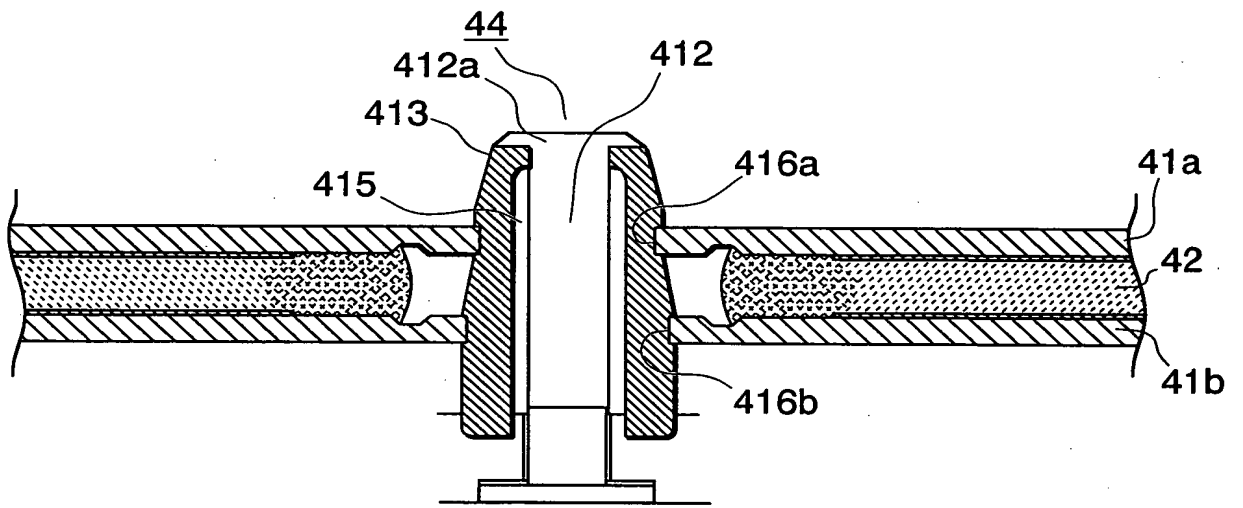


Fig. 24A

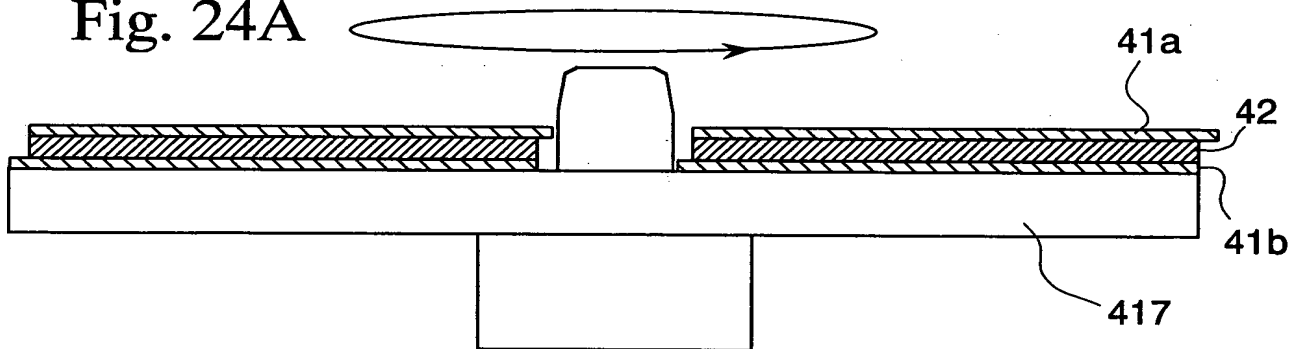


Fig. 24B

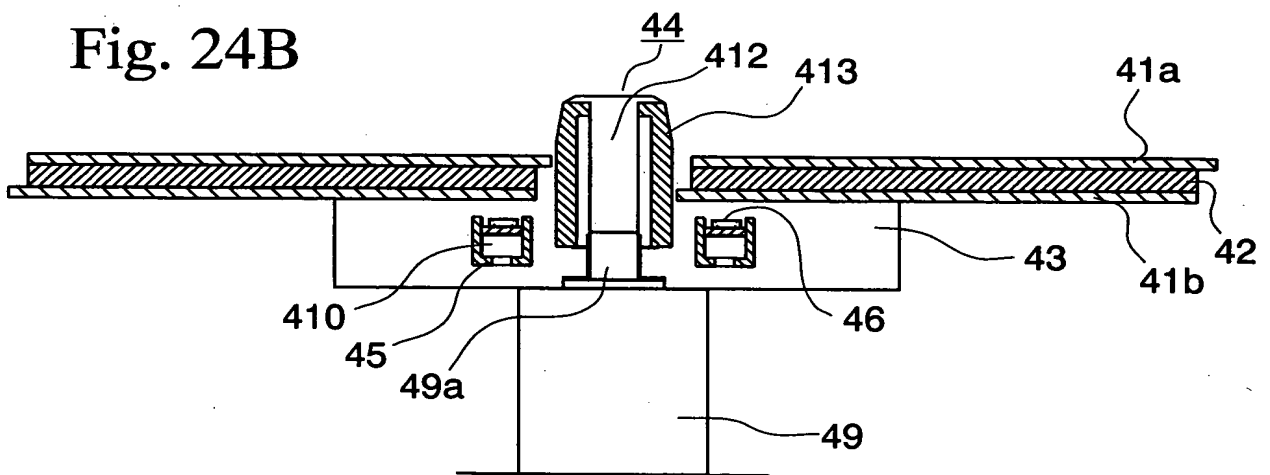




Fig. 24C

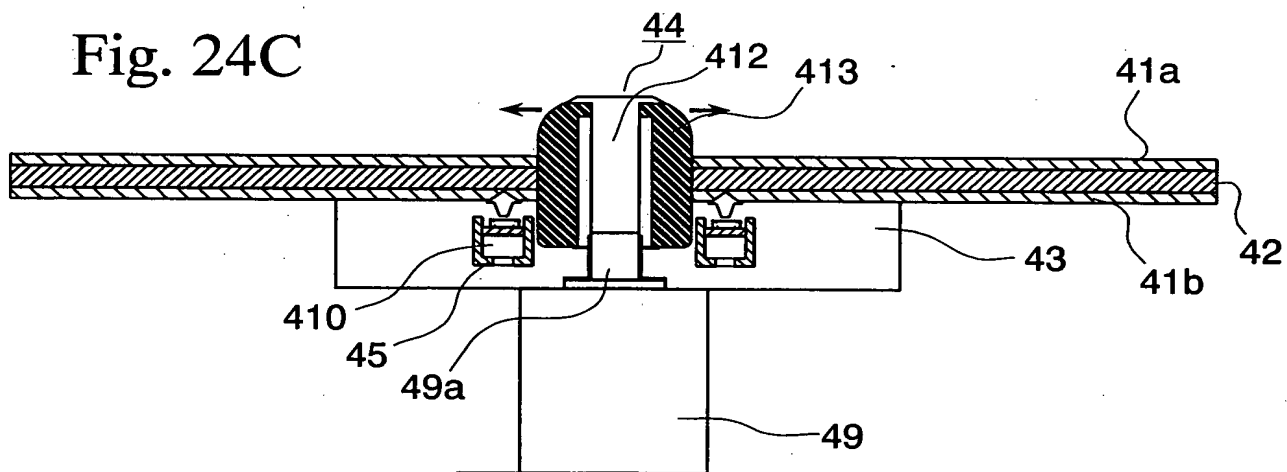


Fig. 24D

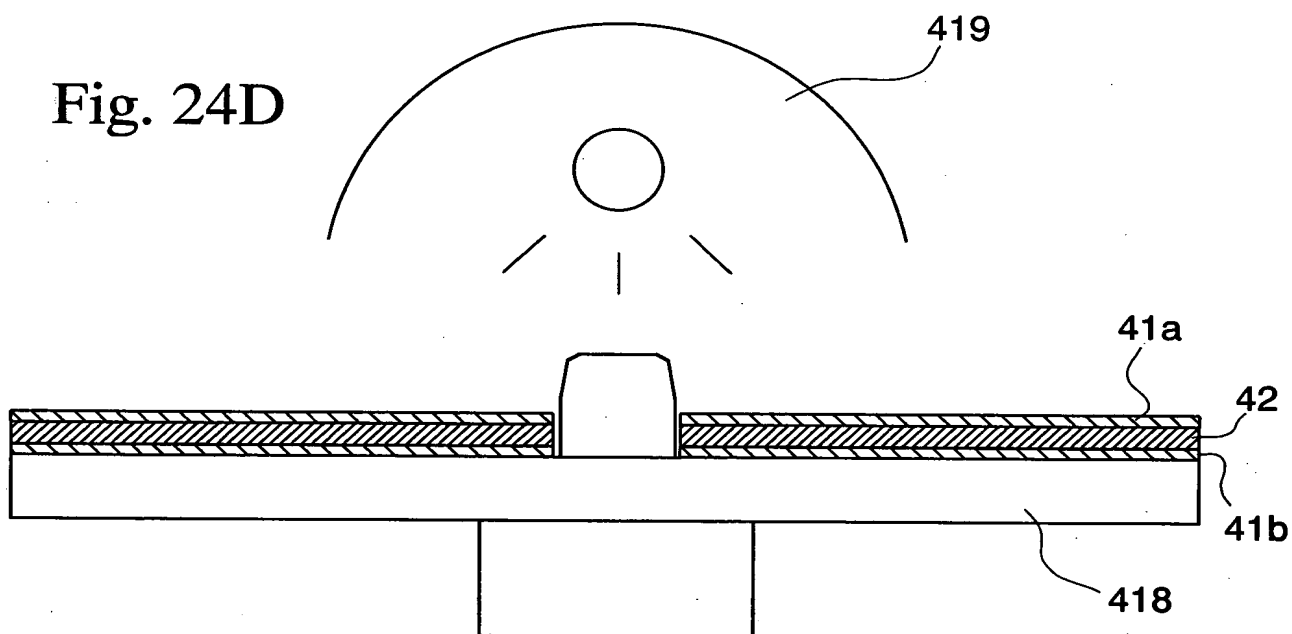


Fig. 25

